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**PATENT**  
**5298-13101/CD02212**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Prather et al.

**Serial No. 10/798,657**

**Filed: March 11, 2004**

**For: LOW DUTY CYCLE DISTORTION  
DIFFERENTIAL TO CMOS  
TRANSLATOR**

**Group Art Unit: 2819**

**Examiner: Vibol Tan**

**Atty. Dkt. No. 5298-13101**

I hereby certify that this correspondence is being transmitted via facsimile or deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 450, Alexandria, VA 22313, on the date indicated below.

08/23/2005  
Date

**Kevin L. Daffer**

**AMENDMENT; RESPONSE TO OFFICE ACTION MAILED MAY 23, 2005**

**Mail Stop Non-Fee Amendment**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313**

**Dear Sir/Madam:**

**Responsive to the Office Action of May 23, 2005, please amend the case as follows:**

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Amendments to the Drawings begin on page 6 of this paper.**

**Remarks begin on page 7 of this paper.**

capacitor, a single inverter, and a single biasing circuit is shown, described, or suggested (Iida -- Fig. 3). In fact, Iida specifically teaches away from replicating the circuit and a double-ended output, since the purpose of Iida is to "provide a level shift circuit which requires a reduced number of circuit elements" compared to that of the prior art circuit of Fig. 1 which has a double-ended output, but absent a biasing circuit and capacitor at each output (Iida -- col. 1, lines 54-56, emphasis added; Figs. 1 and 3 in comparison). Moreover, Iida explicitly states that "it is noted here that the level shift circuit is made up of only capacitor 19, CMOS inverter 20, and the bias circuit or resistor R5" (Iida -- col. 4, lines 18-21, emphasis added). Iida continues by noting the level shifter of Fig. 3, when compared to that shown in Fig. 1, requires less number of circuit elements -- the primary goal of Iida (Iida -- col. 4, lines 22-25).

Accordingly, Applicants do not believe that Iida somehow implicitly suggests two inverters, two capacitors, and two biasing circuits, and simply omits to illustrate such items as suggested by the Examiner. Instead, Iida specifically requires only one of each item in an effort to reduce the number of circuit elements, and also to reduce the current dissipation in its level shifter apparatus. Therefore, one skilled in the art when looking to Iida would not be motivated to increase the circuit elements and the current dissipation by applying a double-ended output if only a single-ended output is suitable and necessitated by the teachings of Iida.

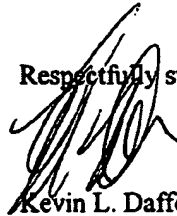
For at least the reasons stated above, Applicants believe independent claim 11 and claims dependent therefrom are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

### **CONCLUSION**

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed May 23, 2005. In view of the remarks herein traversing the rejections, Applicants assert that pending claims 1, 4, 6, 14, and 18 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-13101.

Respectfully submitted,



Kevin L. Daffer  
Reg. No. 34,146  
Attorney for Applicant(s)

Daffer McDaniel, LLP  
P.O. Box 684908  
Austin, TX 78768-4908  
(512) 476-1400  
Date: August 23, 2005

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## PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

Application of Document Number  
10-798,657

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN  
SMALL ENTITY

Column 1		Column 2	SMALL ENTITY		OR	SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.18(a), (b), or (c))							
SEARCH FEE (37 CFR 1.18(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.18(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.18(i))	minus 20 =	*	X	=		X	=
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X	=		X	=
APPLICATION SIZE FEE (37 CFR 1.16(e))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2			TOTAL			TOTAL	

\* If the difference in column 1 is less than zero, enter "0" in column 2

APPLICATION AS AMENDED - PART II

{Column 1}

(Column 2)

(Colour 3)

SMALL ENTITY

Of course,

OTHER THAN  
SMALL ENTITY

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY		SMALL ENTITY	
	Total (37 CFR 1.16(e))	*	Minus	**	=	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X ** =		X * =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIMS (37 CFR 1.16(d))						TOTAL ADD'L FEE		TOTAL ADD'L FEE	

1/11/06

(Colophon 1)

Column 3

6:16:46

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AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(c))	17	Minus	20	—		
Independent (37 CFR 1.16(d))	3	Minus	3	—			
Application Size Fee (37 CFR 1.16(s))							
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIMS							
TOTAL ADJ. FEE							

\* If the entry in column 1 is less than the entry in column 2, write 0 in column 3.

\*\*\* If the "Highest Number Previously Paid For" in THIS SPACE is less than 20, enter:

... If the Highest Number Previously Paid For IN THIS SPACE is less than 2, enter 1

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